

**CERTIFICATE OF TRANSMISSION BY FACSIMILE (37 CFR 1.8)**

Applicant(s): Yasushi Miyajima et al.

Docket No.

YKI-0065

Application No.

09/820,262

Filing Date

03/28/2001

Examiner

Xiao Min Wu

Group Art Unit

2674



Invention: DISPLAY DEVICE OF ACTIVE MATRIX TYPE

I hereby certify that this Amendment Transmittal Letter (1 pg); Response to Office Action (12 pgs)*(Identify type of correspondence)*is being facsimile transmitted to the United States Patent and Trademark Office (Fax. No. 1-703-872-9306)on January 5, 2005*(Date)*

Patricia A. Hart

*(Typed or Printed Name of Person Signing Certificate)**(Signature)*

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<b>AMENDMENT TRANSMITTAL LETTER (Large Entity)</b>					Docket No. <b>YKI-0065</b>	
Applicant(s): <b>Yasushi Miyajima et al.</b>						
Application No. <b>09/820,262</b>	Filing Date <b>03/28/2001</b>	Examiner <b>Xiao Min Wu</b>	Customer No. <b>23413</b>	Group Art Unit <b>2674</b>	Confirmation No. <b>1979</b>	
Invention: <b>DISPLAY DEVICE OF ACTIVE MATRIX TYPE</b>						
						
<u>COMMISSIONER FOR PATENTS:</u>						
Transmitted herewith is an amendment in the above-identified application.						
The fee has been calculated and is transmitted as shown below.						
<b>CLAIMS AS AMENDED</b>						
	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST # PREV. PAID FOR	NUMBER EXTRA CLAIMS PRESENT	RATE	ADDITIONAL FEE	
TOTAL CLAIMS	18 -	22 =	0	x \$50.00	\$0.00	
INDEP. CLAIMS	8 -	3 =	5	x \$200.00	\$1,000.00	
Multiple Dependent Claims (check if applicable) <input type="checkbox"/>					\$0.00	
<b>TOTAL ADDITIONAL FEE FOR THIS AMENDMENT</b>					<b>\$1,000.00</b>	
<input type="checkbox"/> No additional fee is required for amendment. <input checked="" type="checkbox"/> Please charge Deposit Account No. <b>06-1130</b> in the amount of <b>\$1,000.00</b> <input type="checkbox"/> A check in the amount of _____ to cover the filing fee is enclosed. <input checked="" type="checkbox"/> The Director is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account <b>06-1130</b> <input checked="" type="checkbox"/> Any additional filing fees required under 37 C.F.R. 1.16. <input checked="" type="checkbox"/> Any patent application processing fees under 37 CFR 1.17. <input type="checkbox"/> Payment by credit card. Form PTO-2038.						
<b>WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.</b>						
 Daniel F. Drexler Registration No.: 47,535 Customer No.: 23413			Dated: <b>January 5, 2005</b>			
CC:			I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on _____ <div style="text-align: center;">(Date)</div> <div style="text-align: center;">_____ Signature of Person Mailing Correspondence</div> <div style="text-align: center;">_____ Typed or Printed Name of Person Mailing Correspondence</div>			



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

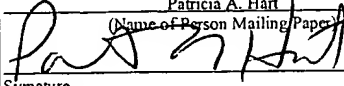
APPLICANT: YASUSHI MIYAJIMA, *et al.* )  
 )  
SERIAL NO: 09/820,262 ) Art Unit: 2674  
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FILED: March 28, 2001 )  
 )  
FOR: DISPLAY DEVICE OF ACTIVE ) Examiner:  
MATRIX TYPE ) Xiao Min Wu  
 )  
 ) Conf. No.: 1979  
 )

**REPLY TO NON-FINAL OFFICE ACTION  
UNDER 37 C.F.R. §1.111, WITH AMENDMENT**

Via Facsimile to 1-703-872-9306  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

In response to the Office Action of October 5, 2004, please enter the following:  
**Amendments to the Claims**, beginning on page 2 of this paper, and  
**Remarks**, beginning on page 11 of this paper.

I hereby certify that this correspondence was facsimile transmitted to the United States Patent Office (Fax No. 1-703-872-9306) on:	
January 5, 2005	
(Date of Deposit)	
Patricia A. Hart	
(Name of Person Mailing Paper)	
	01/05/05
Signature	Date

## AMENDMENT TO THE CLAIMS

Please replace the claims with the following rewritten listing:

1. (Canceled)

2. (Currently Amended) ~~The~~An active matrix type display device ~~comprising:~~according to claim 1

\_\_\_\_\_ a plurality of gate lines;

\_\_\_\_\_ a plurality of data lines crossing said plurality of gate lines;

\_\_\_\_\_ a plurality of pixel electrodes;

\_\_\_\_\_ a thin film transistor disposed at each intersection between said plurality of gate lines and said plurality of data lines, and including a gate electrode and an active region, said gate electrode being connected to one of said plurality of gate lines, and said active region having a first region connected to one of said plurality of data lines and a second region connected to a corresponding one of said plurality of pixel electrodes; and

\_\_\_\_\_ a gate line driver for sequentially applying a gate selection signal with a pulse-shaped voltage waveform to a selected one of said plurality of gate lines; wherein

\_\_\_\_\_ said gate line driver causes a falling edge of said gate selection signal with said pulse-shaped voltage waveform to be smoother than a rising edge thereof;

\_\_\_\_\_ wherein said gate selection signal requires at least a time  $t/2$  to fall, where  $t$  is the time from when a first gate line assumes an unselected state to when subsequent second gate line assumed a selected state.

3. (Canceled)

4. (Currently Amended) ~~The~~An active matrix type display device ~~comprising:~~according to claim 1,

\_\_\_\_\_ a plurality of gate lines;

\_\_\_\_\_ a plurality of data lines crossing said plurality of gate lines;

\_\_\_\_\_ a plurality of pixel electrodes;

\_\_\_\_\_ a thin film transistor disposed at each intersection between said plurality of gate lines and said plurality of data lines, and including a gate electrode and an active region, said gate electrode being connected to one of said plurality of gate lines, and said active region having a first region connected to one of said plurality of data lines and a second region connected to a corresponding one of said plurality of pixel electrodes; and

\_\_\_\_\_ a gate line driver for sequentially applying a gate selection signal with a pulse-shaped voltage waveform to a selected one of said plurality of gate lines; wherein

\_\_\_\_\_ said gate line driver causes a falling edge of said gate selection signal with said pulse-shaped voltage waveform to be smoother than a rising edge thereof;

\_\_\_\_\_ wherein said gate line driver includes a gate buffer provided at a final stage and connected to a corresponding one of said plurality of gate lines,

said gate buffer includes a transistor having first and second regions of an active layer respectively connected to the ground and to said corresponding gate line, and

the condition,  $2.5(R1+R2)*(C1+C2) < t < 5(R1+R2)*(C1+C2)$ , is satisfied, wherein

R1 represents a total resistance of said gate line and the gate electrodes of the thin film transistors connected to said gate line in a pixel region,

C1 represents a total capacitance of capacitors connected to said gate line in the pixel region and having said gate line as one electrode,

R2 represents a channel resistance of the transistor in said gate buffer,

C2 represents a capacitance of a capacitor formed by said active layer of the transistor in said gate buffer and the gate electrode of said transistor, and

t represents a flyback period in a horizontal scanning period.

5. (Original) The active matrix type display device according to claim 4, wherein a channel length L and a channel width W of the transistor in said gate buffer satisfy the condition  $W/L < 1$ .

6. (Currently Amended) ~~The~~An active matrix type display device comprising:  
~~according to claim 1;~~

\_\_\_\_\_ a plurality of gate lines;

\_\_\_\_\_ a plurality of data lines crossing said plurality of gate lines;

\_\_\_\_\_ a plurality of pixel electrodes;

\_\_\_\_\_ a thin film transistor disposed at each intersection between said plurality of gate lines and said plurality of data lines, and including a gate electrode and an active region, said gate electrode being connected to one of said plurality of gate lines, and said active region having a first region connected to one of said plurality of data lines and a second region connected to a corresponding one of said plurality of pixel electrodes; and

\_\_\_\_\_ a gate line driver for sequentially applying a gate selection signal with a pulse-shaped voltage waveform to a selected one of said plurality of gate lines; wherein

\_\_\_\_\_ said gate line driver causes a falling edge of said gate selection signal with said pulse-shaped voltage waveform to be smoother than a rising edge thereof;

\_\_\_\_\_ wherein, said gate line driver includes a gate buffer provided at a final stage and connected to a corresponding one of said plurality of gate lines,

\_\_\_\_\_ said gate buffer includes a transistor having first and second regions of an active layer respectively connected to the ground and to said corresponding gate line, and

\_\_\_\_\_ a channel length L and a channel width W of the transistor in said gate buffer satisfy the condition  $W/L < 1$ .

7. (Currently Amended) ~~The~~An active matrix type display device comprising; according to claim 1,

\_\_\_\_\_ a plurality of gate lines;

\_\_\_\_\_ a plurality of data lines crossing said plurality of gate lines;

\_\_\_\_\_ a plurality of pixel electrodes;

\_\_\_\_\_ a thin film transistor disposed at each intersection between said plurality of gate lines and said plurality of data lines, and including a gate electrode and an active region, said gate electrode being connected to one of said plurality of gate lines, and said active region having a first region connected to one of said plurality of data lines and a second region connected to a corresponding one of said plurality of pixel electrodes; and

\_\_\_\_\_ a gate line driver for sequentially applying a gate selection signal with a pulse-shaped voltage waveform to a selected one of said plurality of gate lines; wherein

said gate line driver causes a falling edge of said gate selection signal with said pulse-shaped voltage waveform to be smoother than a rising edge thereof;

\_\_\_\_\_ wherein, said gate line driver includes a gate buffer provided at a final stage and connected to a corresponding one of said plurality of gate lines,

said gate buffer includes a current supplying transistor having first and second regions of an active layer connected between a power source and said corresponding gate line, and a current discharging transistor having first and second regions of an active layer respectively connected to the ground and to said corresponding gate line, and

the ratio (channel width W) / (channel length L) of said current supplying transistor differs from the ratio (channel width W) / (channel length L) of said current discharging transistor.

8. (Original) The active matrix type display device according claim 7, wherein

the condition,  $2.5(R1+R2)*(C1+C2) < t < 5(R1+R2)*(C1+C2)$  is satisfied wherein

R1 represents a total resistance of said gate line and the gate electrodes of the thin film transistors connected to said gate line in a pixel region,

C1 represents a total capacitance of capacitors connected to said gate line in the pixel region and having said gate line as one electrode,

R2 represents a channel resistance of the current discharging transistor in said gate buffer,

C2 represents a capacitance of a capacitor formed by said active layer of the current discharging transistor in said gate buffer and the gate electrode thereof, and

t represents a flyback period in a horizontal scanning period.

9. (Original) The active matrix type display device according to claim 8, wherein the channel length L and the channel width W of the current discharging transistor in said gate buffer satisfy the condition  $W/L < 1$ .

10. (Original) The active matrix type display device according to claim 8, wherein the condition that the ratio of (the ratio W/L of said current supplying transistor) / (the ratio W/L of said current discharging transistor) is greater than 1 is satisfied.

11. (Original) The active matrix type display device according to claim 8, wherein the condition that the ratio of (the ratio W/L of said current supplying transistor) / (the ratio of said current discharging transistor) is greater than 5 is satisfied.

12. (Canceled)

13. (Currently Amended) ~~The~~An active matrix type display device ~~comprising; according to claim 12~~

\_\_\_\_\_ a plurality of gate lines;

\_\_\_\_\_ a plurality of data lines crossing said plurality of gate lines;

\_\_\_\_\_ a plurality of pixel electrodes;

\_\_\_\_\_ a thin film transistor disposed at each intersection between said plurality of gate lines and said plurality of data lines, and including a gate electrode and an active region, said gate electrode being connected to one of said plurality of gate lines, and said active region having a first region connected to one of said plurality of data lines and a second region connected to a corresponding one of said plurality of pixel electrodes; and

\_\_\_\_\_ a gate line driver for sequentially applying a gate selection signal with a pulse-shaped voltage waveform to a selected one of said plurality of gate lines; wherein

\_\_\_\_\_ said gate line driver causes a falling time of said gate selection signal to be longer than a rising time thereof;

\_\_\_\_\_ wherein said gate selection signal requires at least a time  $t/2$  to fall, where  $t$  is a time from when a first gate line assumes an unselected state to when a subsequent second gate line assumes a selected state.

14. (Canceled)



15. (Currently Amended) ~~The~~An active matrix type display device comprising:  
according to claim 12,

\_\_\_\_\_ a plurality of gate lines;

\_\_\_\_\_ a plurality of data lines crossing said plurality of gate lines;

\_\_\_\_\_ a plurality of pixel electrodes;

\_\_\_\_\_ a thin film transistor disposed at each intersection between said plurality of gate lines and said plurality of data lines, and including a gate electrode and an active region, said gate electrode being connected to one of said plurality of gate lines, and said active region having a first region connected to one of said plurality of data lines and a second region connected to a corresponding one of said plurality of pixel electrodes; and

\_\_\_\_\_ a gate line driver for sequentially applying a gate selection signal with a pulse-shaped voltage waveform to a selected one of said plurality of gate lines; wherein  
\_\_\_\_\_ said gate line driver causes a falling time of said gate selection signal to be longer than a rising time thereof;

\_\_\_\_\_ wherein said gate line driver includes a gate buffer provided at a final stage and connected to a corresponding one of said plurality of gate lines,

said gate buffer includes a transistor having first and second regions of an active layer respectively connected to the ground and to said corresponding gate line, and

the condition,  $2.5(R1+R2)*(C1+C2) < t < 5(R1+R2)*(C1+C2)$ , is satisfied,  
wherein

R1 represents a total resistance of said gate line and the gate electrodes of the thin film transistors connected to said gate line in a pixel region,

C1 represents a total capacitance of capacitors connected to said gate line in the pixel region and having said gate line as one electrode,

R2 represents a channel resistance of the transistor in said gate buffer,

C2 represents a capacitance of a capacitor formed by said active layer of the transistor in said gate buffer and the gate electrode of said transistor, and

t represents a flyback period in a horizontal scanning period.

16. (Original) The active matrix type display device according to claim 15, wherein a channel length L and a channel width W of the transistor in said gate buffer satisfy the condition  $W/L < 1$ .

17. (Currently Amended) ~~The~~An active matrix type display device comprising:  
according to claim 12,

\_\_\_\_\_ a plurality of gate lines;  
\_\_\_\_\_ a plurality of data lines crossing said plurality of gate lines;  
\_\_\_\_\_ a plurality of pixel electrodes;  
\_\_\_\_\_ a thin film transistor disposed at each intersection between said plurality of gate lines and said plurality of data lines, and including a gate electrode and an active region, said gate electrode being connected to one of said plurality of gate lines, and said active region having a first region connected to one of said plurality of data lines and a second region connected to a corresponding one of said plurality of pixel electrodes; and  
\_\_\_\_\_ a gate line driver for sequentially applying a gate selection signal with a pulse-shaped voltage waveform to a selected one of said plurality of gate lines; wherein  
\_\_\_\_\_ said gate line driver causes a falling time of said gate selection signal to be longer than a rising time thereof;  
\_\_\_\_\_ wherein, said gate line driver includes a gate buffer provided at a final stage and connected to a corresponding one of said plurality of gate lines,  
\_\_\_\_\_ said gate buffer includes a transistor having first and second regions of an active layer respectively connected to the ground and to said corresponding gate line, and  
\_\_\_\_\_ a channel length L and a channel width W of the transistor in said gate buffer satisfy the condition  $W/L < 1$ .

18. (Currently Amended) ~~The~~An active matrix type display device comprising:  
according to claim 12,

\_\_\_\_\_ a plurality of gate lines;  
\_\_\_\_\_ a plurality of data lines crossing said plurality of gate lines;  
\_\_\_\_\_ a plurality of pixel electrodes;

a thin film transistor disposed at each intersection between said plurality of gate lines and said plurality of data lines, and including a gate electrode and an active region, said gate electrode being connected to one of said plurality of gate lines, and said active region having a first region connected to one of said plurality of data lines and a second region connected to a corresponding one of said plurality of pixel electrodes; and

a gate line driver for sequentially applying a gate selection signal with a pulse-shaped voltage waveform to a selected one of said plurality of gate lines; wherein

said gate line driver causes a falling time of said gate selection signal to be longer than a rising time thereof;

wherein, said gate line driver included a gate buffer provided at a final stage and connected to a corresponding one of said plurality of gate lines,

said gate buffer includes a current supplying transistor having first and second regions of an active layer connected between a power source and said corresponding gate line, and a current discharging transistor having first and second regions of an active layer respectively connected to the ground and to said corresponding gate line, and

the ratio (channel width W) / (channel length L) of said current supplying transistor differs from the ratio (channel width W) / (channel length L) of said current discharging transistor.

19. (Original) The active matrix type display device according to claim 18, wherein the condition,  $2.5(R1+R2)*(C1+C2) < t < 5(R1+R2)*(C1+C2)$ , is satisfied wherein

R1 represents a total resistance of said gate line and the gate electrodes of the thin film transistors connected to said gate line in a pixel region,

C1 represents a total capacitance of capacitors connected to said gate line in the pixel region and having said gate line as one electrode,

R2 represents a channel resistance of the current discharging transistor in said gate buffer,

C2 represents a capacitance of a capacitor formed by said active layer of the current discharging transistor in said gate buffer and the gate electrode thereof, and

t represents a flyback period in a horizontal scanning period.

20. (Original) The active matrix type display device according to claim 18, wherein the channel length L and the channel width W of the current discharging transistor in said gate buffer satisfy the condition  $W/L < 1$ .

21. (Original) The active matrix type display device according to claim 18, wherein the condition that the ratio of (the ratio W/L of said current supplying transistor) / (the ratio W/L of said current discharging transistor) is greater than 1 is satisfied.

22. (Original) The active matrix type display device according to claim 18, wherein the condition that the ratio of (the ratio W/L of said current supplying transistor) / (the ratio W/L of said current discharging transistor) is greater than 5 is satisfied.

## REMARKS

In an Office Action dated October 5, 2004, the Examiner indicates that pending claims 1, 3, 12 and 14 are rejected as being anticipated over prior art and claims 2, 4-11, 13 and 15-22 are objected to as being dependent upon a rejected base claim, but otherwise contain allowable subject matter.

More specifically, in the present office action, claims 1, 3, 12 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,421,038 to Lee (hereinafter "Lee").

In response, Applicants herein cancel rejected claims 1, 3, 12 and 14. Accordingly, the outstanding rejection is rendered moot; reconsideration and withdrawal thereof is respectfully requested.

Applicants reserve the right to pursue the cancelled claims in an additional application(s) without prejudice in respect of the present claim amendment or otherwise.

As mentioned, the Examiner objects to claims 2, 4-11, 13 and 15-22 but states that these claims would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims. Herein, Applicants amend claims 2, 4-11, 13, and 15-22 to place the claims in condition for allowance.

Particularly, claims 2, 4, 6, and 7 are each rewritten in independent form by encompassing all of the limitations of base claim 1. Accordingly, claims 2, 4 and 6-7, as amended, are novel and non-obvious over the cited references and are thus allowable. Dependent claims 5 and 8-11 variously depend from allowable claims 4 and 7 and are thus correspondingly allowable. Reconsideration and withdrawal of the objections of claims 2 and 4-11 is respectfully requested.

Further, claims 13, 15, 17, and 18 are each rewritten herein in independent form as including all of the limitations of claim 12. Accordingly, claims 13, 15 and 17-18 as amended are novel and non-obvious over the cited reference and are thus allowable. Dependent claims 16 and 19-22 variously depend from allowable claims 15 and 18 and

are thus correspondingly allowable. Reconsideration and withdrawal of the objections of claims 13 and 15-22 is respectfully requested.

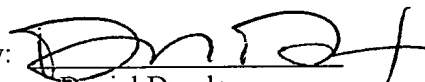
All of the objections and rejections are herein overcome. No new matter is added by way of the present Amendments and Remarks as support is found throughout the originally filed specification, claims and drawings. The application is now allowable to Applicants. Prompt issuance of Notice of Allowance is requested.

The Examiner is invited to contact Applicant's attorney at the below-listed phone number regarding this Response or otherwise concerning the present application.

If there are any charges due with respect to this Amendment or otherwise, please charge them to Deposit Account No. 06-1130 maintained by Applicant's attorneys.

Respectfully submitted,  
CANTOR COLBURN LLP

By:



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Date: JAN. 05-2004